AMENDMENTS TO THE DRAWINGS:

The attached replacement sheet of drawings includes changes to Fig. 4 and replaces the previous replacement sheet including Fig. 4.

Figure 4 was amended to label reference 30, amend Figure 1 to Figure 3, extend the reference box for CM2 to include transistors QM3 to QMN, extend reference box CM1 to include transistor QIN1, and to label current source IOC.

Attachments following last page of this Amendment:

Replacement Sheet (1 page)

REMARKS

Claims 1 to 11 and 13 are pending in this application of which claims 1, 6 and 9 are the independent claims. Favorable reconsideration and further examination are respectfully requested.

Applicant thanks the Examiner for conducting an interview on Monday, July 25, 2005. The Examiner indicated that he would allow claim 1 if the Applicant amended claim 1 to indicate that the impedance divider was directly connected to the supply voltage source to include the positive and negative terminals.

Initially, the Examiner objected to the use of the terms "compensation circuit" and "current output", if these terms are the same thing or if different, these terms are not clearly differentiated. Applicant believes the Examiner was actually referring to "compensation current" instead of "compensation circuit." Applicant has amended claim 1 to eliminate this alleged ambiguity.

The Examiner also objected to FIG. 4 because reference 30 was not labeled. Applicant has amended FIG. 4 to label reference 30. Applicant respectfully requests removal of the drawing objection.

Turning to the art rejections, claims 1 to 11 and 13 were rejected under 35 U.S.C. § 102(b) as being anticipated by Nomura et al. (U.S. Patent No. 5,675,280).

Claim 1, as amended, is directed to a current compensation circuit. The compensation circuit includes an impedance divider directly coupled to a supply voltage source of a current

mirror circuit and the impedance divider coupled to ground. The impedance driver includes an output node. The impedance divider is configured to generate a compensation signal at the output node representative of voltage changes in the supply voltage source. The compensation circuit also includes a common-source gain stage having a stage input coupled to the output node and a stage output connected to a node of the current mirror circuit. The gain stage is configured to generate a compensation current from the stage output for application to the node of the current mirror circuit in response to the compensation signal. The common-source gain stage includes a first parallel array of programmable transistors for defining a predetermined range of the compensation current.

The applied art is not understood to disclose or suggest the foregoing features of claim 1. In particular, Nomura does not disclose or suggest an impedance divider directly coupled to a supply voltage source of a current mirror circuit and coupled to ground.

Specifically, Nomura discloses a load circuit 27, which the Examiner has equated to an impedance driver that is not directly coupled to VCC, the supply voltage of the current mirror 66 and 67. In fact, when looking at Figure 5, load circuit 27 is separated from VCC by constant current source circuit 22. The Examiner has further stated in the 25 July teleconference that Nomura is directly connected to VCC through the ground. Applicant respectfully disagrees. One skilled in art would understand that being directly coupled to a supply voltage source would not refer to being directly connected to ground but referring to being directly coupled to VCC, which is the supply voltage source.

Furthermore, Nomura does not disclose or suggest a common-source gain stage having a stage input coupled to the output node and a stage output connected to a node of the current mirror circuit. The Examiner has indicated that the "common-source gain stage" is represented in Nomura as circuit 57, but he has also indicated that the current mirror circuit reads on the combination of FETs 66 and 67 (page 4 of the Office Action). However, FETs 66 and 67 are included within circuit 57 (see FIG. 5 of Nomura). Therefore, Nomura does not disclose or suggest that the common-source gain stage having a stage input coupled to the output node and a stage output connected to a node of the current mirror circuit.

Applicant respectfully requests withdrawal of the art rejection.

Claims 6 and 9 have corresponding features to claim 1. Applicant submits that claims 6 and 9 are patentable for at least the same reasons as claim 1. Applicant submits that all dependent claims now depend on allowable independent claims.

For at least the foregoing reasons, Applicant requests withdrawal of the art rejection.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Applicant submits that the entire application is now in condition for allowance. Such action is respectfully requested at the Examiner's earliest convenience.

All correspondence should be directed to the address below. Applicant's attorney can be reached by telephone at (617) 422-3532.

No fee is believed to be due for this Response; however, if any fees are due, please apply such fees to Deposit Account No. 20-0515 referencing Attorney Docket 1847-US.

Respectfully submitted,

Date: 26 July 2005

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